CLAIMS

What is claimed is:

1   1.   A capacitor array in an integrated circuit, the capacitor
2   array comprising:
3   a plurality of dummy unit capacitor cells decoupled from
4   signal paths to provide visual symmetry;
5   a plurality of active unit capacitor cells having a
6   terminal coupled to signal paths carrying analog signals; and
7   wherein the plurality of active unit capacitor cells is
8   arranged in the capacitor array with the dummy unit capacitor
9   cells to provide visual symmetry and electrical symmetry.

1   2.   The capacitor array of claim 1 wherein,
2   the electrical symmetry to provide electrical matching
3   between active unit capacitor cells, and
4   the visual symmetry to provide process environment
5   uniformity.

1   3.   The capacitor array of claim 1 wherein,
2   the visual symmetry is provided by
3   selecting the same size and shape of capacitor plates
4   for each unit capacitor in the capacitor array, and
5   uniformly spacing each unit capacitor in the capacitor
6   array;
7   and wherein
8   the electrical symmetry is provided by
9   arranging the plurality of active unit capacitors
10   amongst the plurality of dummy unit capacitors in the

11   capacitor array so that the far range fringing fields are

12   symmetric.

1   4.   A capacitor array in an integrated circuit, the capacitor

2 array comprising:

3   a plurality of unit capacitor cells arranged to provide

4 visual symmetry;

5   a set of N active unit capacitor cells of the plurality of

6 unit capacitor cells having a terminal coupled to a signal path

7 to carry analog signals;

8   if N is a prime number, arranging the N active unit

9 capacitor cells to be symmetrically located to form an N-

10 equilateral two-dimensional shape to provide electrical

11 symmetry,

12   otherwise if N is not a prime number,

13   dividing the set of N active unit capacitor cells into

14   P subsets of M active unit capacitor cells, arranging the M

15   active unit capacitor cells of each of the P subsets to be

16   symmetrically located to form an M-equilateral two-

17   dimensional shape in a neighborhood, and

18   separating each neighborhood of each M-equilateral

19   two-dimensional shape by one or more dummy unit capacitor

20   cells to avoid encroachment of one neighborhood into

21   another in order to provide electrical symmetry.

1   5.   The capacitor array of claim 4 wherein,

2   the plurality of unit capacitor cells are arranged in

3 equally spaced apart rows and columns to provide visual

4 symmetry.

1 6.   The capacitor array of claim 4 wherein,

2   the electrical symmetry to provide electrical matching

3 between active unit capacitor cells, and

4   the visual symmetry to provide process environment

5 uniformity.

1 7.   The capacitor array of claim 4 wherein,

2   the N-equilateral shape is slightly skewed, and

3   a predetermined distance of separation is maintained

4 between active cells.

1 8.   The capacitor array of claim 4 wherein,

2   the unit capacitor cells are integrated circuit capacitors.

1 9.   The capacitor array of claim 8 wherein,

2   the integrated circuit capacitors are metal oxide

3 semiconductor capacitors.

1 10.   The capacitor array of claim 8 wherein,

2   the integrated circuit capacitors are thin film capacitors.

1 11.   A method in an integrated circuit comprising:

2   arranging a plurality of dummy unit capacitors and a

3 plurality of active unit capacitors in a capacitor array to

4 provide visual symmetry;

5   further arranging the plurality of dummy unit capacitors
6   and the plurality of active capacitors in the capacitor array to
7   provide electrical symmetry;
8   wherein the dummy unit capacitors are decoupled from signal
9   paths; and
10   wherein the active unit capacitors have at least one
11   terminal coupled to a signal path carrying an analog signal.

1   12.   The method of claim 11 wherein,
2   the electrical symmetry to provide electrical matching
3   between active unit capacitors, and
4   the visual symmetry to provide process environment
5   uniformity.

1   13.   The method of claim 11 wherein,
2   the visual symmetry is provided by
3   selecting the same size and shape of capacitor plates
4   for each unit capacitor in the capacitor array, and
5   uniformly spacing each unit capacitor in the capacitor
6   array.

1   14.   The method of claim 11 wherein,
2   the electrical symmetry is provided by
3   arranging the plurality of active unit capacitors
4   amongst the plurality of dummy unit capacitors in the
5   capacitor array so that the far range fringing fields are
6   symmetric.

1   15.   The method of claim 11 wherein,

2   the method is a layout method defining mask layers for the

3   manufacture of a capacitor array in the integrated circuit.

1   16. A computer program product for layout of a capacitor array

2   in an integrated circuit, comprising:

3   a computer usable medium having

4   computer readable program code to arrange a plurality

5   of dummy unit capacitors and a plurality of active unit

6   capacitors in a capacitor array to provide visual symmetry,

7   and

8   computer readable program code to arrange the

9   plurality of active capacitors amongst the plurality of

10   dummy unit capacitors in the capacitor array to provide

11   symmetric far range fringing fields to each of the

12   plurality of active capacitors;

13   and

14   wherein the dummy unit capacitors are decoupled from signal

15   paths and the active unit capacitors have at least one terminal

16   coupled to a signal path carrying an analog signal.

1   17. The computer program product of claim 16 wherein,

2   the visual symmetry is provided by

3   selecting the same size and shape of capacitor plates

4   for each unit capacitor in the capacitor array, and

5   uniformly spacing each unit capacitor in the capacitor

6   array.

1   18. The computer program product of claim 16 wherein,

2   the computer usable medium further has

3 computer readable program code to define the mask layers of
4 a unit capacitor of the capacitor array.

1 19. The computer program product of claim 16 wherein,
2   the computer usable medium is a semiconductor medium, a
3 magnetic medium, an optical medium, or a processor readable
4 medium.

1 20. The computer program product of claim 16 wherein,
2   the computer usable medium is a computer data signal
3 embodied in a carrier wave over a transmission medium.

1 21. An N-bit digital to analog converter (DAC) with a binary-
2 weighted capacitor ladder in an integrated circuit, the N-bit
3 DAC comprising:
4   N-1 sampling switches each having a control gate, a first
5 pole, and a second pole coupled to a voltage reference;
6   a switch controller to receive an N-bit digital data input
7 signal and generate N-1 control signals, the N-1 control signals
8 respectfully coupled to each control gate of the N-1 sampling
9 switches to switch the N-1 sampling switches open and closed in
10 response to the N-bit digital data input signal;
11   N capacitors formed out of a plurality of active unit
12 capacitor cells in a capacitor array, each of the N capacitors
13 having a top capacitor plate coupled together and to an output
14 of the binary-weighted capacitor ladder, one of the N capacitors
15 having a bottom capacitor plate coupled to a ground while the
16 remaining N-1 capacitors have a bottom capacitor plate
17 respectively coupled to each first pole of the N-1 sampling
18 switches; and

19   wherein the plurality of active unit capacitor cells to
20   form the N capacitors being arranged with a plurality of dummy
21   unit capacitor cells in the capacitor array to provide visual
22   symmetry and electrical symmetry.

1   22.   The N-bit DAC of claim 21 wherein,
2   the integrated circuit is a digital to analog converter.

1   23.   The N-bit DAC of claim 21 wherein,
2   the integrated circuit is an analog to digital converter
3   and the N-bit DAC is a portion of each stage of the analog to
4   digital converter to successively approximate the analog input
5   signal.

1   24.   The N-bit DAC of claim 21 wherein
2   the electrical symmetry to provide electrical matching
3   between active unit capacitors, and
4   the visual symmetry to provide process environment
5   uniformity.

1   25.   The N-bit DAC of claim 21 wherein
2   the visual symmetry is provided by
3   selecting the same size and shape of capacitor plates
4   for each unit capacitor in the capacitor array, and
5   uniformly spacing each unit capacitor in the capacitor
6   array.

1   26.   The N-bit DAC of claim 21 wherein

2 the electrical symmetry is provided by

3 arranging the plurality of active unit capacitors

4 amongst the plurality of dummy unit capacitors in the

5 capacitor array so that the far range fringing fields are

6 symmetric.

1 27. The N-bit DAC of claim 21 wherein

2 the electrical symmetry is provided by

3 if a number M of active unit capacitor cells forming the

4 capacitor is a prime number, arranging the M active unit

5 capacitor cells to be symmetrically located to form an M-

6 equilateral two dimensional shape to provide electrical

7 symmetry,

8 otherwise if M is not a prime number,

9 dividing the set of M active unit capacitor cells into

10 P subsets of Q active unit capacitor cells, arranging the Q

11 active unit capacitor cells of each of the P subsets to be

12 symmetrically located to form an Q-equilateral two

13 dimensional shape in a neighborhood, and

14 separating each neighborhood of each Q-equilateral

15 two-dimensional shape by one or more dummy unit capacitor

16 cells to avoid encroachment of one neighborhood into

17 another.

1 28. The N-bit DAC of claim 21 further comprising:

2 N grounding switches each having a control gate, a first

3 pole, and a second pole coupled to the ground;

4 and

5 wherein one of the N grounding switches has the first

6 pole coupled to the output;

7 wherein the remaining N-1 capacitors have their bottom
8 capacitor plate respectively coupled to each first pole of
9 the remaining N-1 grounding switches; and
10 wherein the switch controller to further generate N
11 inverted control signals, the N inverted control signals
12 respectfully coupled to each control gate of the N
13 grounding switches to switch the N grounding switches open
14 and closed in response to the N-bit digital data input
15 signal.

1 29. An N-bit digital to analog converter (DAC) with an equally-
2 weighted capacitor array in an integrated circuit, the N-bit DAC
3 comprising:
4 a first plurality of N switches each having a switch
5 control gate, a first pole, and a second pole, the second pole
6 of each of the first plurality of N switches coupled to a low
7 level voltage supply;
8 a second plurality of N switches each having a switch
9 control gate, a first pole, and a second pole, the second pole
10 of each of the second plurality of N switches coupled to a
11 voltage reference, the first pole of each of the second
12 plurality of N switches coupled respectively to the
13 corresponding first pole of the first plurality of N switches;
14 a digital input signal having N control signals, each of
15 the N control signals coupled respectively to each switch
16 control gate of the first plurality of N switches and coupled
17 respectively to each switch control gate of the second plurality
18 of N switches, the N control signals to switch the second
19 plurality of N switches open and closed and to switch the first
20 plurality of N switches closed and open, respectively, in
21 response to the digital input signal;

22   N capacitors formed out of a plurality of active unit

23   capacitor cells in a capacitor array, each of the N capacitors

24   having a top capacitor plate coupled together and to an analog

25   output of the DAC, the N capacitors each have a bottom capacitor

26   plate respectively coupled to each first pole of the first

27   plurality of N switches and each first pole of the second

28   plurality of N switches; and

29   wherein the plurality of active unit capacitor cells to

30   form the N capacitors being arranged with a plurality of dummy

31   unit capacitor cells in the capacitor array to provide visual

32   symmetry and electrical symmetry to provide a substantial

33   equally matched capacitance for each of the N capacitors.

1   30. The N-bit DAC of claim 29 wherein,

2   the integrated circuit is a digital to analog converter.

1   31. The N-bit DAC of claim 29 wherein,

2   the integrated circuit is an analog to digital converter

3   and the N-bit DAC is a portion of each stage of the analog to

4   digital converter to successively approximate the analog input

5   signal.

1   32. The N-bit DAC of claim 29 wherein

2   the electrical symmetry to provide electrical matching

3   between active unit capacitors, and

4   the visual symmetry to provide process environment

5   uniformity.

1   33. The N-bit DAC of claim 29 wherein

2   the visual symmetry is provided by

3   selecting the same size and shape of capacitor plates

4   for each unit capacitor in the capacitor array, and

5   uniformly spacing each unit capacitor in the capacitor

6   array.

1   34. The N-bit DAC of claim 29 wherein

2   the electrical symmetry is provided by

3   arranging the plurality of active unit capacitors

4   amongst the plurality of dummy unit capacitors in the

5   capacitor array so that the far range fringing fields are

6   symmetric.

1   35. The N-bit DAC of claim 29 wherein

2   the electrical symmetry is provided by

3   if a number M of active unit capacitor cells forming the

4   capacitor is a prime number, arranging the M active unit

5   capacitor cells to be symmetrically located to form an M-

6   equilateral two dimensional shape to provide electrical

7   symmetry,

8   otherwise if M is not a prime number,

9   dividing the set of M active unit capacitor cells into

10   P subsets of Q active unit capacitor cells, arranging the Q

11   active unit capacitor cells of each of the P subsets to be

12   symmetrically located to form an Q-equilateral two

13   dimensional shape in a neighborhood, and

14   separating each neighborhood of each Q-equilateral

15   two-dimensional shape by one or more dummy unit capacitor

16   cells to avoid encroachment of one neighborhood into

17   another.

1 36. The N-bit DAC of claim 29 wherein
2   the first plurality of N switches are n-channel field
3 effect transistors; and
4   the second plurality of N switches are p-channel field
5 effect transistors.

1 37. The N-bit DAC of claim 36 wherein
2   the digital input signal is a thermometer coded digital
3 input signal, and
4   each of the N control signals are directly coupled
5 respectively to each switch control gate of the n-channel field
6 effect transistors and are directly coupled respectively to each
7 switch control gate of the p-channel field effect transistors.

1 38. The N-bit DAC of claim 29 wherein
2   the N control signals include N positive control signals
3 and N negative control signals,
4   each of the N positive control signals are directly coupled
5 respectively to each switch control gate of the first plurality
6 of N switches, and
7   each of the N negative control signals are directly coupled
8 respectively to each switch control gate of the second plurality
9 of N switches.

1 39. The N-bit DAC of claim 38 wherein
2   the N negative control signals are respective inverted
3 logical signals of the N positive control signals.

1 40. The N-bit DAC of claim 29 further comprising:

2   a switch controller to receive the digital input signal and

3 generate the N control signals in response thereto.

1 41. The N-bit DAC of claim 40 wherein

2   the N control signals include N positive control signals

3 and N negative control signals,

4   each of the N positive control signals are directly coupled

5 respectively to each switch control gate of the first plurality

6 of N switches, and

7   each of the N negative control signals are directly coupled

8 respectively to each switch control gate of the second plurality

9 of N switches.

1 42. The N-bit DAC of claim 41 wherein

2   the N negative control signals are respective inverted

3 logical signals of the N positive control signals.

1 43. A pipelined analog to digital converter (ADC) in an

2 integrated circuit to receive an analog input signal and to

3 generate a digital output signal, the pipelined analog to

4 digital converter (ADC) comprising:

5   a plurality of M converter stages coupled in series

6 together, each of the M converter stages to receive an analog

7 input and generate an analog residue output, each of the

8 plurality of M converter stages including

9   a K-bit flash analog to digital converter to receive

10   the analog input and generate a stage digital output,

11   wherein K is a variable from stage to stage over the

12   plurality of M converter stages;

13   an N-bit digital to analog converter (DAC) with an

14   equally-weighted capacitor array, the N-bit DAC to receive

15   the stage digital output to generate an estimated analog

16   output, the N-bit DAC including

17   a first plurality of N switches each having a

18   switch control gate, a first pole, and a second pole,

19   the second pole of each of the first plurality of N

20   switches coupled to a first voltage reference,

21   a second plurality of N switches each having a

22   switch control gate, a first pole, and a second pole,

23   the second pole of each of the second plurality of N

24   switches coupled to a second voltage reference, the

25   first pole of each of the second plurality of N

26   switches coupled respectively to the corresponding

27   first pole of the first plurality of N switches,

28   wherein the stage digital output has N control

29   signals, each of the N control signals coupled

30   respectively to each switch control gate of the first

31   plurality of N switches and coupled respectively to

32   each switch control gate of the second plurality of N

33   switches, the N control signals to switch the second

34   plurality of N switches open and closed and to switch

35   the first plurality of N switches closed and open,

36   respectively, in response to the stage digital output,

37   N capacitors formed out of a plurality of active

38   unit capacitor cells in a capacitor array, each of the

39   N capacitors having a top capacitor plate coupled

40   together and to the estimated analog output, the N

41   capacitors each have a bottom capacitor plate

42   respectively coupled to each first pole of the first

43   plurality of N switches and each first pole of the

44   second plurality of N switches,

45   wherein the plurality of active unit capacitor

46   cells to form the N capacitors being arranged with a

47   plurality of dummy unit capacitor cells in the

48   capacitor array to provide visual symmetry and

49   electrical symmetry to provide a substantial equally

50   matched capacitance for each of the N capacitors, and

51   wherein N is a variable from stage to stage over

52   the plurality of M converter stages;

53   and,

54   an analog subtractor to receive the analog input and

55   subtract the estimated analog output therefrom to generate

56   the analog residue output.

1   44. The pipelined analog to digital converter (ADC) of claim 43

2   wherein

3   the analog subtractor includes an amplifier to amplify the

4   magnitude of analog residue output.

1   45. The pipelined analog to digital converter (ADC) of claim 43

2   wherein

3   a first converter stage of the plurality of M converter

4   stages to receive the analog input signal of the analog to

5   digital converter (ADC) as the analog input,

6   and the analog to digital converter (ADC) further includes

7   a digital bit corrector to receive each stage digital

8   output of the respective plurality of M converter stages

9   and to generate the digital output signal of the analog to

10   digital converter in response to the analog input signal.

1 46. The pipelined analog to digital converter (ADC) of claim 43

2 further comprising:

3   a last converter stage coupled in series with an Mth

4 converter stage of the plurality of M converter stages, the last

5 converter stage including

6   an J-bit flash analog to digital converter to receive

7   the analog residue output of the Mth converter stage as the

8   analog input and generate a last stage digital output.

1 47. The pipelined analog to digital converter (ADC) of claim 46

2 wherein

3   a first converter stage of the plurality of M converter

4 stages to receive the analog input signal of the analog to

5 digital converter (ADC) as the analog input,

6   and the analog to digital converter (ADC) further includes

7   a digital bit corrector to receive each stage digital

8   output of the respective plurality of M converter stages

9   and the last stage digital output of the last converter

10   stage to generate the digital output signal of the analog

11   to digital converter in response to the analog input

12   signal.

1 48. The pipelined analog to digital converter (ADC) of claim 43

2 wherein

3   the N-bit DAC in each of the plurality of M converter

4   stages further includes

5   a switch controller to receive the digital input

6   signal and generate the N control signals in response

7   thereto.

1   49. The pipelined analog to digital converter (ADC) of claim 43
2   wherein
3   the first voltage reference is a negative voltage
4   reference and
5   the second voltage reference is a positive voltage
6   reference.

1   50. The pipelined analog to digital converter (ADC) of claim 43
2   wherein
3   the first voltage reference is a low level voltage
4   supply.

1   51. The pipelined analog to digital converter (ADC) of claim 43
2   wherein
3   the low level voltage supply is ground.

1   52. The pipelined analog to digital converter (ADC) of claim 43
2   wherein
3   the N-bit DAC in each of the plurality of M converter
4   stages further includes
5   a third plurality of N switches each having a
6   switch control gate, a first pole, and a second pole,
7   the second pole of each of the second plurality of N
8   switches coupled to a low level voltage supply, the
9   first pole of each of the third plurality of N
10   switches coupled respectively to the corresponding
11   first pole of the first plurality of N switches.

1 53. The pipelined analog to digital converter (ADC) of claim 52
2 wherein
3   the switch control gates of the third plurality
4   of switches are coupled together and to a reset
5   control signal to close each of the third plurality of
6   switches and initialize the N capacitors of the
7   capacitor array.

1 54. A pipelined analog to digital converter (ADC) in an
2 integrated circuit to receive an analog input signal and to
3 generate a digital output signal, the pipelined analog to
4 digital converter (ADC) comprising:
5   a plurality of converter stages coupled in series together,
6 each of the plurality of converter stages including
7   a flash analog to digital converter to receive the
8   analog input and generate a stage digital output;
9   a digital to analog converter (DAC) with a capacitor
10   array, the digital to analog converter to receive the stage
11   digital output to generate an estimated analog output, the
12   digital to analog converter including
13   a plurality of switches each having a switch
14   control gate, a first pole, and a second pole,
15   a plurality of active unit capacitor cells in the
16   capacitor array, each of the active unit capacitor
17   cells having a capacitor plate coupled to each
18   respective first pole of the plurality of switches,
19   respectively,
20   wherein the plurality of active unit capacitor
21   cells to form the active capacitors being arranged
22   with a plurality of dummy unit capacitor cells in the

23   capacitor array to provide visual symmetry and

24   electrical symmetry to provide a substantial equally

25   matched capacitance for each of the active unit

26   capacitors.

1   55. The pipelined analog to digital converter (ADC) of claim 54

2   wherein

3   the electrical symmetry to provide electrical matching

4   between active unit capacitors, and

5   the visual symmetry to provide process environment

6   uniformity.

1   56. The pipelined analog to digital converter (ADC) of claim 54

2   wherein

3   the visual symmetry is provided by

4   selecting the same size and shape of capacitor plates

5   for each unit capacitor in the capacitor array, and

6   uniformly spacing each unit capacitor in the capacitor

7   array.

1   57. The pipelined analog to digital converter (ADC) of claim 54

2   wherein

3   the electrical symmetry is provided by

4   arranging the plurality of active unit capacitors

5   amongst the plurality of dummy unit capacitors in the

6   capacitor array so that the far range fringing fields are

7   symmetric.

1 58. The pipelined analog to digital converter (ADC) of claim 54

2 wherein

3   the electrical symmetry is provided by

4   if a number M of active unit capacitor cells forming the

5 active capacitor is a prime number, arranging the M active unit

6 capacitor cells to be symmetrically located to form an M-

7 equilateral two dimensional shape to provide electrical

8 symmetry,

9   otherwise if M is not a prime number,

10   dividing the set of M active unit capacitor cells into

11   P subsets of Q active unit capacitor cells, arranging the Q

12   active unit capacitor cells of each of the P subsets to be

13   symmetrically located to form an Q-equilateral two

14   dimensional shape in a neighborhood, and

15   separating each neighborhood of each Q-equilateral

16   two-dimensional shape by one or more dummy unit capacitor

17   cells to avoid encroachment of one neighborhood into

18   another.

1 59. The pipelined analog to digital converter (ADC) of claim 54

2 wherein

3   a bottom capacitor plate is the capacitor plate of each of

4 the active capacitors which is coupled to each respective first

5 pole of the plurality of switches.

1 60. A pipelined analog to digital converter (ADC) in an

2 integrated circuit to receive an analog input signal and to

3 generate a digital output signal, the pipelined analog to

4 digital converter (ADC) comprising:

5   a plurality of converter stages coupled in series together,

6 each of the plurality of converter stages including

7   a flash analog to digital converter to receive the

8 analog input and generate a stage digital output;

9   a multiplying digital to analog converter (MDAC) with

10 a capacitor array, the digital to analog converter to

11 receive the stage digital output to generate a residual

12 analog output, the multiplying digital to analog converter

13 including

14   a first plurality of switches each having a

15   switch control gate, a first pole, and a second pole,

16   the second pole of each of the first plurality of

17   switches coupled together and to a negative reference

18   voltage,

19   a second plurality of switches each having a

20   switch control gate, a first pole, and a second pole,

21   the second pole of each of the second plurality of

22   switches coupled together and to a positive reference

23   voltage, each first pole of the second plurality of

24   switches correspondingly coupled to each first pole of

25   the first plurality of switches, respectively.

26   a third plurality of switches each having a

27   switch control gate, a first pole, and a second pole,

28   each second pole of the third plurality of switches

29   corresponding coupled to each first pole of the first

30   plurality of switches and each first pole of the

31   second plurality of switches, respectively,

32   a fourth plurality of switches each having a

33   switch control gate, a first pole, and a second pole,

34   the second pole of each of the fourth plurality of

35   switches coupled together and to an analog input,

36   a plurality of active capacitors in the capacitor

37   array each having a first capacitor plate and a second

38   capacitor plate, each first capacitor plate of the
39   active capacitors coupled to each first pole of the
40   third plurality of switches and each first pole of the
41   fourth plurality of switches, respectively, each
42   second capacitor plate of each of the active
43   capacitors coupled together,
44   an operational amplifier having an input coupled
45   to each second capacitor plate of each of the active
46   capacitors, the operational amplifier to generate the
47   analog residue output,
48   a switch having a switch control gate, a first
49   pole, and a second pole, the first pole of the switch
50   coupled to input of the operational amplifier and the
51   second capacitor plate of each of the active
52   capacitors, the second pole of the switch coupled to
53   the analog residue output of the operational
54   amplifier, and
55   wherein a plurality of active unit capacitor
56   cells form the active capacitors and are arranged with
57   a plurality of dummy unit capacitor cells in the
58   capacitor array to provide visual symmetry and
59   electrical symmetry to provide a substantial equally
60   matched capacitance for each of the active capacitors.

1   61.   The pipelined analog to digital converter (ADC) of claim 60
2   wherein
3   the multiplying digital to analog converter further
4   includes
5   a fifth plurality of switches each having a
6   switch control gate, a first pole, and a second pole,
7   the second pole of each of the fifth plurality of
8   switches coupled together and to a low level power

9   supply voltage, each first pole of the fifth plurality

10   of switches correspondingly coupled to each first pole

11   of the first plurality of switches and to each first

12   pole of the second plurality of switches,

13   respectively.

1   62. The pipelined analog to digital converter (ADC) of claim 61

2   wherein

3   the low level power supply voltage is ground.

1   63. The pipelined analog to digital converter (ADC) of claim 61

2   wherein

3   the multiplying digital to analog converter further

4   includes

5   a sixth plurality of switches each having a

6   switch control gate, a first pole, and a second pole,

7   the second pole of each of the sixth plurality of

8   switches coupled together and to the analog residue

9   output, each first pole of each of the sixth plurality

10   of switches coupled to each first capacitor plate of

11   the active capacitors, each first pole of the third

12   plurality of switches, and each first pole of the

13   fourth plurality of switches, respectively.

1   64. The pipelined analog to digital converter (ADC) of claim 60

2   wherein

3   the electrical symmetry to provide electrical matching

4   between active unit capacitors, and

5   the visual symmetry to provide process environment

6   uniformity.

1 65. The pipelined analog to digital converter (ADC) of claim 60

2 wherein

3   the visual symmetry is provided by

4   selecting the same size and shape of capacitor plates

5   for each unit capacitor in the capacitor array, and

6   uniformly spacing each unit capacitor in the capacitor

7   array.

1 66. The pipelined analog to digital converter (ADC) of claim 60

2 wherein

3   the electrical symmetry is provided by

4   arranging the plurality of active unit capacitors

5   amongst the plurality of dummy unit capacitors in the

6   capacitor array so that the far range fringing fields are

7   symmetric.

1 67. The pipelined analog to digital converter (ADC) of claim 60

2 wherein

3   the electrical symmetry is provided by

4   if a number M of active unit capacitor cells forming the

5 active capacitor is a prime number, arranging the M active unit

6 capacitor cells to be symmetrically located to form an M-

7 equilateral two dimensional shape to provide electrical

8 symmetry,

9   otherwise if M is not a prime number,

10   dividing the set of M active unit capacitor cells into

11   P subsets of Q active unit capacitor cells, arranging the Q

12   active unit capacitor cells of each of the P subsets to be

13   symmetrically located to form an Q-equilateral two

14   dimensional shape in a neighborhood, and

15   separating each neighborhood of each Q-equilateral

16   two-dimensional shape by one or more dummy unit capacitor

17   cells to avoid encroachment of one neighborhood into

18   another.